AD 622

DATA ACQUISITION CARD

USER'S MANUAL

HUMUSOFT®

Printed in Czech Republic

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1. Introduction

1.1. General Description

The AD 622 data acquisition card is designed for the need of connecting PC compatible computers to real world signals. The AD 622 contains 8 channel fast 14 bit A/D converter with simultaneous sample/hold circuit, 8 independent 14 bit D/A converters, 8 bit digital input port and 8 bit digital output port. The card is designed for standard data acquisition and control applications and optimized for use with Real Time Toolbox for Simulink®. AD 622 features fully 32 bit architecture for fast throughput.

1.2. Features List

The AD 622 offers following features:

- 32-bit architecture
- 14 bit A/D converter with simultaneous sample & hold circuit
- Conversion time 1.6 µs for single channel or 3.7 µs for 8 channels
- 8 channel single ended fault protected input multiplexer
- Input range ±10V
- Internal clock & voltage reference
- 8 D/A converters with 14 bit resolution and ±10V output range
- 8 bit TTL compatible digital input port
- 8 bit TTL compatible digital output port
- Interrupt

- Requires one PCI 2.3 slot and optional second slot for second connector
- Can be used in 5V or 3.3V slot
- Power consumption 500 mA@+5V, 150 mA@+12V, 150 mA@-12V
- Operating temperature 0°C to +70°C

1.3. Specifications

1.3.1. A/D Converter

Resolution:	14 bits
Number of channels:	8 single ended
Sample/hold circuit:	simultaneous sampling of all channels
Conversion time:	1.6 µs single channel
	1.9 µs 2 channels
	2.5 µs 4 channels
	3.7 µs 8 channels
FIFO:	8 entries/one conversion cycle
Input ranges:	±10V
Input protection:	±18V
Input impedance:	> 10^{10} Ohm

1.3.2. D/A Converter

Resolution:	14 bit
Number of channels:	8
Settling time:	max. 31 µs (full scale swing, 1/2 LSB)
Slew Rate:	10 V/µs
Output current:	min. ±10 mA
Short circuit current:	±15 mA

DC output impedance:	max. 0.5 Ohm
Load capacitance:	max. 50 pF
Differential nonlinearity:	±1 LSB

1.3.3. Digital Inputs

Number of bits:	8
Input signal levels:	TTL
Logic 0:	0.8 V max.
Logic 1:	2.0 V min.

1.3.4. Digital Outputs

Number of bits:	8
Output signal levels:	TTL
Logic 0:	0.5 V max. @ 24 mA (sink)
Logic 1:	2.0 V min. @ 15 mA (source)
Outputs:	TTL

2. Installation

2.1. Board Installation

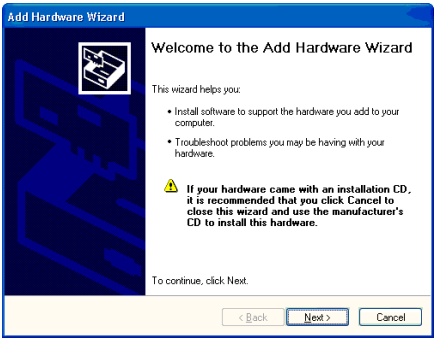
AD 622 has no switches or jumpers and you can install it in any free PCI expansion slot of your computer. Follow the steps outlined below:

- Turn off the power of the computer system and unplug the power cord.
- Disconnect all cables connected to the computer system.
- Using a screwdriver, remove the cover-mounting screws. These screws are at the rear side of the PC.
- Remove the computer system's cover.
- Find an empty expansion slot in your computer for AD 622 card. If the slot still has the metal expansion-slot cover attached, remove the cover with a screwdriver. Save the screw to install the AD 622.
- Hold the AD 622 firmly at the top of the board, and press the gold edge connector into an empty PCI expansion slot.
- Using a screwdriver, screw the retaining bracket tightly against the rear plate of the computer system.
- In case of using also quadrature encoder inputs or timer/counters install also the aditional connector with metal slot cover to the neighbouring slot. Otherwise you can disconnect the aditional connector from the board and save it for future use.
- Replace the cover of the computer, and plug in the power cord.
- Reconnect all cables that were previously attached to the rear of the computer.

2.2. Driver Installation

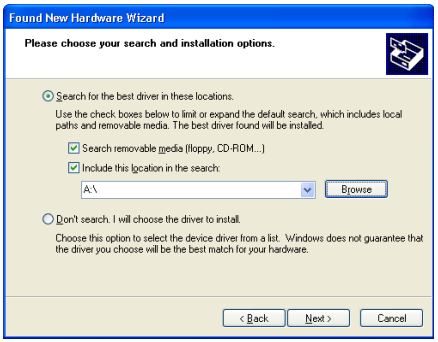
Once you have installed AD 622 to PCI slot you can install Windows driver. Follow the steps outlined below:

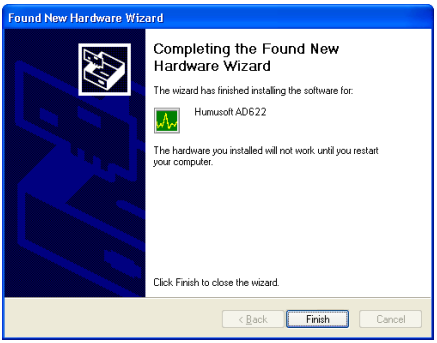
Turn on the computer, boot Microsoft Windows. AD 622 is detected by system automatically. In Add Hardware Wizzard window click Next.



Insert installation floppy into drive a. In Found New Hardware Wizzard select Install the software automatically and click Next.

When prompted for driver location type a:\ and click Next. Click Finish to complete installation.





3. Programming Guide

3.1. Register Map

AD 622 uses PCI Vendor ID 0x186C and Device ID 0x0622. Registers of AD 622 card are located in 3 memory mapped regions:

Region	**Function**	**Size (bytes)**	**Width (bits)**
BADR0 (memory mapped)	PCI chipset, interrupts, status bits, special functions	32	32
BADR1 (memory mapped)	A/D, D/A, digital I/O	128	16/32

Table 1. Base Address Regions

PCI chipset (PCI 9030) and counter/timer chip are located in 32-bit regions and should be accessed by 32-bit instructions. BADR1 containing analog I/O has 16-bit architecture and registers are naturally 16-bit wide, but 32-bit access to this area is allowed as well under certain conditions. 32-bit access is broken by PCI chipset into two 16-bit cycles on the AD 622 internal bus. This allows increasing throughput by accessing two consecutive internal 16-bit registers by single PCI cycle. Therefore two D/A channels can be written or two A/D channels can be read at once which increases speed of data transfers almost twice. Do not use 32-bit access to other registers than ADDATA and DA0 - DA7.

Address	Read	Write
BADR0+0x4C	**INTCSR**	**INTCSR**
BADR0+0x54	**GPIOC**	**GPIOC**

Table 2. BADR0 Memory Map

Address	Read	Write
BADR1+0x00	**ADDATA** - A/D data	**ADCTRL** - A/D control
BADR1+0x02	**ADDATA** - A/D data mirror	
BADR1+0x04	**ADDATA** - A/D data mirror	
BADR1+0x06	**ADDATA** - A/D data mirror	
BADR1+0x08	**ADDATA** - A/D data mirror	
BADR1+0x0A	**ADDATA** - A/D data mirror	
BADR1+0x0C	**ADDATA** - A/D data mirror	
BADR1+0x0E	**ADDATA** - A/D data mirror	
BADR1+0x10	**DIN** - Digital input	**DOUT** - Digital output
BADR1+0x20	**ADSTART** - A/D SW trigger	**DA0** - D/A 0 data
BADR1+0x22		**DA1** - D/A 1 data
BADR1+0x24		**DA2** - D/A 2 data
BADR1+0x26		**DA3** - D/A 3 data
BADR1+0x28		**DA4** - D/A 4 data
BADR1+0x2A		**DA5** - D/A 5 data
BADR1+0x2C		**DA6** - D/A 6 data
BADR1+0x2E		**DA7** - D/A 7 data

Table 3. BADR1 Memory Map

3.2. Register Description

INTCSR **BADR0+0x4C** **Interrupt Control/Status** **R/W**

Bit	Description	Default
0	**ADINT Enable**. 1 enables A/D interrupt, 0 disables A/D interrupt.	0
1	**ADINT Polarity**. 1 active high, 0 active low. Connected to **EOLC** of A/D converter, should be set to active low for normal operation.	0
2	**ADINT Status**. 1 indicates interrupt active, 0 indicates interrupt not active.	0
5:3	Reserved.	0
6	**PCI Interrupt Enable**. 1 enables PCI interrupt.	0
7	**Software Interrupt**. 1 generates PCI interrupt (INTA#) if PCI Interrupt Enable bit is set (bit [6]=1).	0
8	**ADINT Select Enable**. 1 indicates edge triggered, 0 indicates level triggered interrupt. ***Note:*** *Operates only in High-Polarity mode (bit [1]=1)*	0
9	Reserved.	0
10	**ADINT Clear**. Writing 1 to this bit clears ADINT in edge mode.	0
31:11	Reserved	0x000600

Table 4. INTCSR - Interrupt Control/Status Register Format

GPIOC BADR0+0x54 Genaral Purpose I/O Control R/W

Bit	Description	Default
16:0	Reserved.	0x006C0
17	**EOLC**. Reads EOLC (end of last conversion) bit of A/D converter. Active low, 0 when all channels converted, 1 during A/D conversion.	0
21:18	Reserved.	0x10
23	**LDAC**. Load D/A converters, active low. Writing 0 makes A/D latches transparent, 1 holds D/A outputs. Can be used for simultaneous update of analog outputs.	0
25:24	Reserved.	10
26	**DACEN**. 1 enables D/A outputs. 0 forces 0V to all D/A outputs.	0
31:27	Reserved.	0

Table 5. GPIOC - General Purpose I/O Control Register Format

ADCTRL BADR1+0x00 A/D Control W

Bit	Description	Default
0	**CH0 select**. 1 enables chanel 0 in channel scan list.	0
1	**CH1 select**. 1 enables chanel 1 in channel scan list.	0
2	**CH2 select**. 1 enables chanel 2 in channel scan list.	0
3	**CH3 select**. 1 enables chanel 3 in channel scan list.	0
4	**CH4 select**. 1 enables chanel 4 in channel scan list.	0
5	**CH5 select**. 1 enables chanel 5 in channel scan list.	0
6	**CH6 select**. 1 enables chanel 6 in channel scan list.	0
7	**CH7 select**. 1 enables chanel 7 in channel scan list.	0
15:8	Reserved.	0x00

Table 6. ADCTRL - A/D Control Register Format

ADDATA BADR1+0x00 A/D Data R

Bit	Description	Default
13:0	**A/D Data.** Reads data from A/D. Data is valid after EOLC bit in GPIOC goes low. Data from channels selected in ADCTRL register are available in FIFO, lower number channels first.	N/A
15:14	Reserved	N/A

Table 7. ADDATA - A/D DATA Register Format

Note: *ADDATA register has 7 mirror registers located from BADR1+0x02 to BADR1+0x0E. This arrangement remaps FIFO to linear address space and allows reading consecutive values from A/D FIFO by 32-bit instructions.*

DIN BADR1+0x10 Digital Input R

Bit	Description	Default
7:0	**Digital input 7:0.** Reads digital input port.	1
15:8	Reserved	N/A

Table 8. DIN - Digital Input Register Format

DOUT BADR1+0x10 Digital Output W

Bit	Description	Default
7:0	**Digital output 7:0.** Writes to digital output port.	0
15:8	Reserved	N/A

Table 9. DOUT - Digital Output Register Format

ADSTART BADR1+0x20 A/D Conversion Start R

Bit	Description	Default
15:0	**A/D Conversion Start.** Reading this register triggers A/D conversion for all channels selected in ADCTRL.	N/A

Table 10. ADSTART - A/D Conversion Start Register Format

DA0	**BADR1+0x20**	**D/A Converter 0**	**W**
DA1	**BADR1+0x22**	**D/A Converter 1**	**W**
DA2	**BADR1+0x24**	**D/A Converter 2**	**W**
DA3	**BADR1+0x26**	**D/A Converter 3**	**W**
DA4	**BADR1+0x28**	**D/A Converter 4**	**W**
DA5	**BADR1+0x2A**	**D/A Converter 5**	**W**
DA6	**BADR1+0x2C**	**D/A Converter 6**	**W**
DA7	**BADR1+0x2E**	**D/A Converter 7**	**W**

Bit	Description	Default
13:0	**DAx**. D/A converter channel n data.	0x3FFF
15:14	Reserved.	N/A

Table 12. DAx - D/A Converter Data Register Format

Note: *D/A converter outputs are updated only if LDAC bit in GPIOC registrer is set low (bit [23] at BADR0+0x54 =0). Otherwise D/A outputs are keeping old values and data written to DAn registers are kept until LDAC goes low. LDAC bit can be used for simultaneous update of D/A outputs.*

3.3. A/D Converter

A/D converter is controlled through ADDATA, ADCTRL, ADSTART and GPIOC registers.

Before starting a conversion it is necessary to configure channels which will be converted by ADCTRL register. Each A/D channel has one bit in ADCTRL. Setting this bit includes the channel in conversion scan list. Conversion can be initiated by a read operation from ADSTART register. Once the conversion is started, selected channels are simultaneously sampled and converted. When the conversion of all selected channels is complete, EOLC (bit 17 in GPIOC register) is set low which means that converted data is available in output FIFO and can be read from ADDATA register. EOLC remains low until next conversion is started. Starting

new conversion resets FIFO.

A/D converter has fixed input range ±10V and uses two's complement binary coding. A/D converter zero offset can be adjusted by R23. A/D gain can be adjusted by R25.

Digital Value	**Analog Voltage**
0x3FFF	-0.0012 V
0x2000	-10.0000 V
0x1FFF	9.9988 V
0x0000	0.0000 V

Table 13. A/D Inputs Coding

3.4. D/A Converters

D/A converters are accessed through eight data input latch registers DA0 - DA7. D/A converter outputs are initially connected to ground until DACEN (bit 26 in GPIOC register) is set to 1. This bit can be used to disconnecting all analog outputs from D/A converters. Data from D/A input latch registers are passed to D/A converters only if LDAC (bit 23 in GPIOC register) is 0. If this bit is set to 1, data remains just in input latches without being written to D/A converters. Then if LDAC is set to 0, all D/A outputs are updated simultaneously from input latch registers.

Output voltage ranges of D/A converters are ±10V and straight binary coding is used. After power-on or hardware reset the output voltage is set to 0V. D/A converter positive range can be adjusted by R5 while negative range can be adjusted by R8.

Digital Value	Analog Voltage
0x3FFF	9.9988 V
0x2000	0.0000 V
0x1FFF	-0.0012 V
0x0000	-10.0000 V

Table 14. D/A Outputs Coding

3.5. Digital I/O

MF 624 contains one 8-bit digital input port and one 8-bit digital output port. Digital input port can be accessed directly by read from DIN register. Inputs are TTL compatible. Digital output port can be accessed by byte or word write to DOUT register. Outputs are TTL compatible. After power-on or hardware reset digital outputs are set to 0.

4. I/O Signals

4.1. Output Connector Signal Description

The AD 622 multifunction I/O card is equipped with an on-board 37 pin D-type female connector X1. For pin assignment refer to Table 15. TB 620 Terminal Board can be connected to X1 connector.

AD0-AD7	Analog inputs
DA0-DA7	Analog outputs
DIN0-DIN7	TTL compatible digital inputs
DOUT0-DOUT7	TTL compatible digital outputs
+12V	+12V power supply
-12V	-12V power supply
+5V	+5V power supply
AGND	Analog ground
GND	Digital ground

AD0	**1**	**20**	DA0
AD1	**2**	**21**	DA1
AD2	**3**	**22**	DA2
AD3	**4**	**23**	DA3
AD4	**5**	**24**	DA4
AD5	**6**	**25**	DA5
AD6	**7**	**26**	-12V
AD7	**8**	**27**	+12V
AGND	**9**	**28**	+5V
DA6	**10**	**29**	GND
DA7	**11**	**30**	DOUT0
DIN0	**12**	**31**	DOUT1
DIN1	**13**	**32**	DOUT2
DIN2	**14**	**33**	DOUT3
DIN3	**15**	**34**	DOUT4
DIN4	**16**	**35**	DOUT5
DIN5	**17**	**36**	DOUT6
DIN6	**18**	**37**	DOUT7
DIN7	**19**		

Table 15. X1 Connector Pin Assignement

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